David Gogiberidze

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EDUCATION

Pennsylvania State University *Aug 2021—May 2025*
Bachelor of Science in Computer Engineering (University Park, PA)
*GPA: **3.73***

SKILLS

Languages: Java, Python, C#, C, Unix, SQL, Verilog/System Verilog, Assembly, MIPS

Hardware Design: MultiSIM, LTSpice, Vivado, Altium Designer, KiCad, Cadence Virtuoso, Quartus Prime.

RELEVANT COURSES

Data Structures & Algorithms, Computer Architecture, OS programing, BJTS/MOSFETS, Signals and Systems, Statistics, Communication Networks, Digital Integrated Circuit Design, Embedded/Micro Systems, Systems Debugging

PROJECT EXPERIENCE

High-Quality USB Audio Digital-Analog Converter *May 2024—Sep 2024*

USB DAC implementing the PCM1792A supporting up to 192KHz/24-bit audio playback

- Created the schematic and laid out a 4-layer PCB with minimal susceptibility to noise, incorporating power planes, ground planes, and signal isolation with optimal component placement to ensure high audio quality.
- Designed an Op Amp filtering stage to convert differential analog current outputs to a 2V RMS line out.
- Developed firmware for the XU316 microcontroller in C to function as a USB to I2S transceiver and I2C master
- Utilized I2C to interface with the CS2100 PLL Synthesizer, enabling low jitter system clock support for sampling frequencies from 44.1KHz to 192KHz.

Five Stage MIPS CPU *Aug 2023—Dec 2023*

Five stage CPU written in Verilog with Vivado that supports 32-bit MIPS instructions

- Architected and implemented a five-stage pipelined CPU in Verilog within AMD Vivado, supporting a reduced 32-bit MIPS instruction set.
- Created modules for essential CPU components, including multiplexers, an ALU, control units, and registers.
- Designed comprehensive testbenches and test cases to validate MIPS instruction functionality and correctness, using waveform analysis for accurate verification.
- Integrated forwarding and hazard detection mechanisms to address pipeline hazards, reduce stalls and improve instruction throughput.

Dynamic Out-of-Order CPU Scheduling Simulator *Jan 2024—May 2024*

Accepts an input list of RISC instructions and outputs the cycle that an instruction will be completed

- Developed a cycle-accurate pipelined CPU simulator in Python that implements O-o-O scheduling with conservative load-store ordering implementing register renaming using a free list.
- Modeled important CPU stages: Fetch, Decode, Rename, Dispatch, Issue, Writeback, Commit and handled dependencies that might occur between stages.
- Designed the simulator to process up to 256 instructions with a configurable issue width and number of physical registers.

WORK EXPERIENCE

Systems Engineering Intern | Exelon *June 2023—Aug 2024*

ComED Renewable Energy Advanced Control and Telemetry Systems Engineer

- Developed the front end of an internal data management tool using HTML, CSS, and JavaScript.
- Collaborated with team members using git and fixed bugs to enhance user experience and data reporting accuracy.
- Utilized Power BI to create interactive dashboards and reports that displayed metrics and trends from an internal database.
- Presented data collection tools in team meetings to demonstrate functionality, gather feedback, and drive continuous improvement.